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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Complete if Known

Application Number	10/768,558
Filing Date	January-29, 2004
First Named Inventor	Christopher Hamlin
Group Art Unit	2825
Examiner Name	S. Whitmore
Attorney Docket No.	103-2099

Sheet 1 of 1

## U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code (if known)			
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W		20030005401		Shmuel Winer	01-02-2003	
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Examiner signature	<i>W</i>	Date considered	8/3/05
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1/29/04

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Serial No.:

**LIST OF PATENTS AND PUBLICATIONS FOR  
APPLICANT'S INFORMATION DISCLOSURE  
STATEMENT**

Applicant:

Christopher Hamlin, et al.

Filing Date:

January 29, 2004

Group:

Atty. Docket No.: 03-2099

EXAMINER NAME: S. Whitmore

Reference Designation

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner

Initial

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AW ABA "Layout Compaction in Digital Circuits," by Prof. Kurt Keutzer and A.R. Newton, EECS, University of California, Berkeley, CA; Implication of Deep Submicron, Simplex Solutions; © 1997, A. Richard Newton; 16 pages; [www-cad.eecs.berkeley.edu/HomePages/keutzer/classes/ee244fa98/lectures/ee2443\\_2/ee2443\\_2.pdf](http://www-cad.eecs.berkeley.edu/HomePages/keutzer/classes/ee244fa98/lectures/ee2443_2/ee2443_2.pdf).

AW ACA "Layout Compaction for Yield Optimization Via Critical Area Minimization," by Youcef Bourai and C.-J. Richard Shi, Electrical Engineering Department, University of Washington, Box 352500, Seattle, Washington 98195; 4 pages; [http://jamaica.ee.pitt.edu/Archives/ProceedingArchives/Date/Date2000/papers/2000/date00/pdffiles/02c\\_4.pdf](http://jamaica.ee.pitt.edu/Archives/ProceedingArchives/Date/Date2000/papers/2000/date00/pdffiles/02c_4.pdf).

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AW AGA "Layout Synthesis Techniques for Yield Enhancement," by Venkat K.R. Chiluvuri and Israel Koren, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, MA 01003; 21 pages; <http://citeseer.ist.psu.edu/cachedpage/90278/1>. Originally published in *IEEE Trans. on Semiconductor Manufacturing*, Vol. 8, Special Issue on Defect, Fault, and Yield Modeling, pp. 178-187, May 1995.

Examiner:

Date Considered:

EXAMINER: Initial if reference considered, whether nor not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.